INTERFACE

FOR BALL-EFRATOM* RUBIDIUM FREQUENCY STANDARD

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KCBS-TV RUBIDIUM ATOMIC FREQUENCY STANDARD

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SPECIFICATIONS

KCBS-TV Rubidium Atomic Frequency Standard Support Chassis

Input Power 120 VAC 60 Hz and/or 28 VDC

Current Consumption:

D.C.

Startup 1.8 amps

Run .8 amps

A.C.

Startup .5 amps

Run .17 amps

Outputs

2 BNC front panel.

#1 = 1 MHz. square wave, 1 volt P-P, 75 ohms source Z.

#2 = 10 MHz. square wave, 1 volt P-P, 75 ohms source Z.

4 BNC rear of buffer/divider card.

#1-3 = 1 MHz. square wave, 1 volt P-P, 75 ohms source Z.

#4 = 10 MHz. square wave, 1 volt P-P, 75 ohms source Z.

One set dry contacts to drive external alarm. These contacts are closed when the unit is operating normally and locked, and open at all other times. They appear at TB-1, terminals 1 and 2.

For all other specifications, see Ball Efratom Division manual on the M-100 standard, or the Acopian power supply book for the B28GT110 supply.

RUBIDIUM ATOMIC STANDARD SUPPORT CHASSIS
Description

The support chassis provides a physical mounting for the Ball Efratom Division M-100 rubidium atomic standard assembly, it's A.C. power supply, and the KCBS-designed interface card. It also provides for external alarm connections, and provides metering for the various voltages found in the M-100 standard, and the two supply voltages.

Upon referring to the schematic, it will be seen that the design is relatively straight-forward and is largely self-explanatory.

The two 1N5408 diodes are power supply steering diodes, allowing connection of external 28 volts D.C. to create a dual redundant power supply.

R1 and R2 are each made up of two resistors selected in test to produce 303 to 304 K ohms total.

Relay K1 is a dry contact pair to the Ronan alarm, and is held closed by conduction of a transistor inside the M-100 unit when the standard has internal lock.

The front-panel L.E.D. is a local indication of the same lock condition, and is lit when the standard is locked.

The A.C. power supply is provided with it's own fuse on it's rear panel, and therefore there is no additional fuse protection in the support chassis. It is intended that the unit be supplied with un-interruptable A.C. power to ensure reliability. The unit should be supplied with a 2 amp breaker from the external 28 volt D.C. source to provide over-current protection for the external supply.

ATOMIC FREQUENCY STANDARD
BUFFER AND DIVIDER CARD
Theory of Operation

The Buffer and Divider card provides buffered outputs from the rubidium frequency standard. There are a total of six outputs. Two are at the Rb standard frequency (10 MHz.) and four are at a frequency of Rb/10 (1 MHz.). One of the 1 MHz. outputs and one of the 10 MHz. outputs are available at front panel BNC jacks. The remaining outputs are available on BNC jacks mounted on an aluminum bracket affixed to the rear of the Buffer and Divider card.

The Rb frequency standard module outputs a 10 MHz. sine wave with an amplitude of .5 volt RMS. In order to provide multiple outputs to the various items of equipment in the KCBS plant that require a 1 MHz. standard, it was necessary to both buffer and to divide the output from the Rb standard. In order to preserve the high accuracy of the Rb atomic standard, special measures were taken in the design of the Buffer and Divider card to minimize the addition of phase and duty cycle errors to the signal as it is processed.

In order to divide the signal by 10, and to simplify the design of the buffer, it was necessary to convert the Rb standard sine wave output into a square wave. Because this portion of the signal processing is the most likely to introduce phase errors, a highly accurate zero-crossing detector was designed to do this job.

U1 is a high-speed comparator. The input 10 MHz. sine wave is capacitively coupled to the non-inverting input of U1 at pin 2. Pin 2 is also D.C. biased via R1 and R2 to be approximately half way between VCC and ground, or 2.5 volts. The non-inverting input of U1 at pin 3

is supplied with a voltage which is integrated from the waveform at the Q output of U1 at pin 7. The integration is accomplished by R3, C3, R4, and C4.

It is important to understand the operation of this circuit, because it's proper functioning is crucial to minimizing errors in the zero-crossing detection process. U1 functions similarly to an operational amplifier operated open-loop. When the non-inverting input voltage rises above the inverting input voltage, the Q output rails to VCC, and the not-Q output rails to ground. When the non-inverting input voltage falls below the inverting input voltage, the Q and not-Q states are reversed, i.e. Q is ground, and not-Q is VCC.

In order to provide for a 50% duty-cycle output, consistent phase delay over time, and consistently accurate detection of the actual zero-crossing points of the input sine wave, it is crucial that the inverting input be at the same average voltage as the non-inverting input. This is accomplished by integrating the output of the detector and using the resultant voltage as the comparison voltage applied to the inverting input of U1, as described above.

Should the D.C. value of the input sine wave zero axis deviate from the current comparison voltage applied to U1's inverting input (for example, in the positive direction), the amount of time that the non inverting input is positive with respect to the inverting input will increase from a nominal 50% of the time to some greater value. When this happens, the detector output square wave exceeds a 50% duty cycle, i.e. the positive half of the square wave will be longer in duration than the zero half. (The square wave alternates between 5 volts and zero volts.) Therefore, the voltage that results from integrating the Q output of U1 will be in excess of 50% of VCC.

(Remember that 50% of VCC is the nominal value of the D.C. bias applied to the non-inverting input, and hence should be close to the zero axis of the input sine wave, barring disturbances.) This means that the non-inverting input of U1 will rise to the same D.C. value as the new axis of the input sine wave, resulting in a restoration of 50% duty cycle conditions.

Should the input sine wave's zero axis deviate in the negative direction (with respect to the inverting input voltage), the positive peak of the sine wave will be shorter in time duration than the negative peak. As a result, the output square wave appearing at the Q output will have a less than 50% duty cycle, resulting in a lower voltage out of the integrator. This again will restore equilibrium conditions to the D.C. inputs to U1.

This negative feedback circuit is necessary to compensate for changes in input signal level to the comparator, changes in R1 or R2, or any other disturbances that may arise.

From this point on, the circuit is relatively straightforward. The 10 MHz. square-wave output of the zero-crossing detector is applied to two of the inverters in U3, to become buffered 10 MHz. outputs, and also to programmable divider U2. The 1 MHz. output of U2 is applied to the remaining inverters in U3 to provide 1 MHz. buffered square-wave outputs. R5 through R10 are 75 ohm build-out resistors to establish a standard output impedance for all outputs. This allows distribution of the signals throughout the plant via 75 ohm coax. Because of internal current-limiting in the SN7404 hex inverter, the maximum voltage that can be realized at the 75 ohm outputs is 1 volt peak.

Capacitors C2, C5, and C6 provide transient suppression at the VCC pins of U1, U3, and U2 respectively.

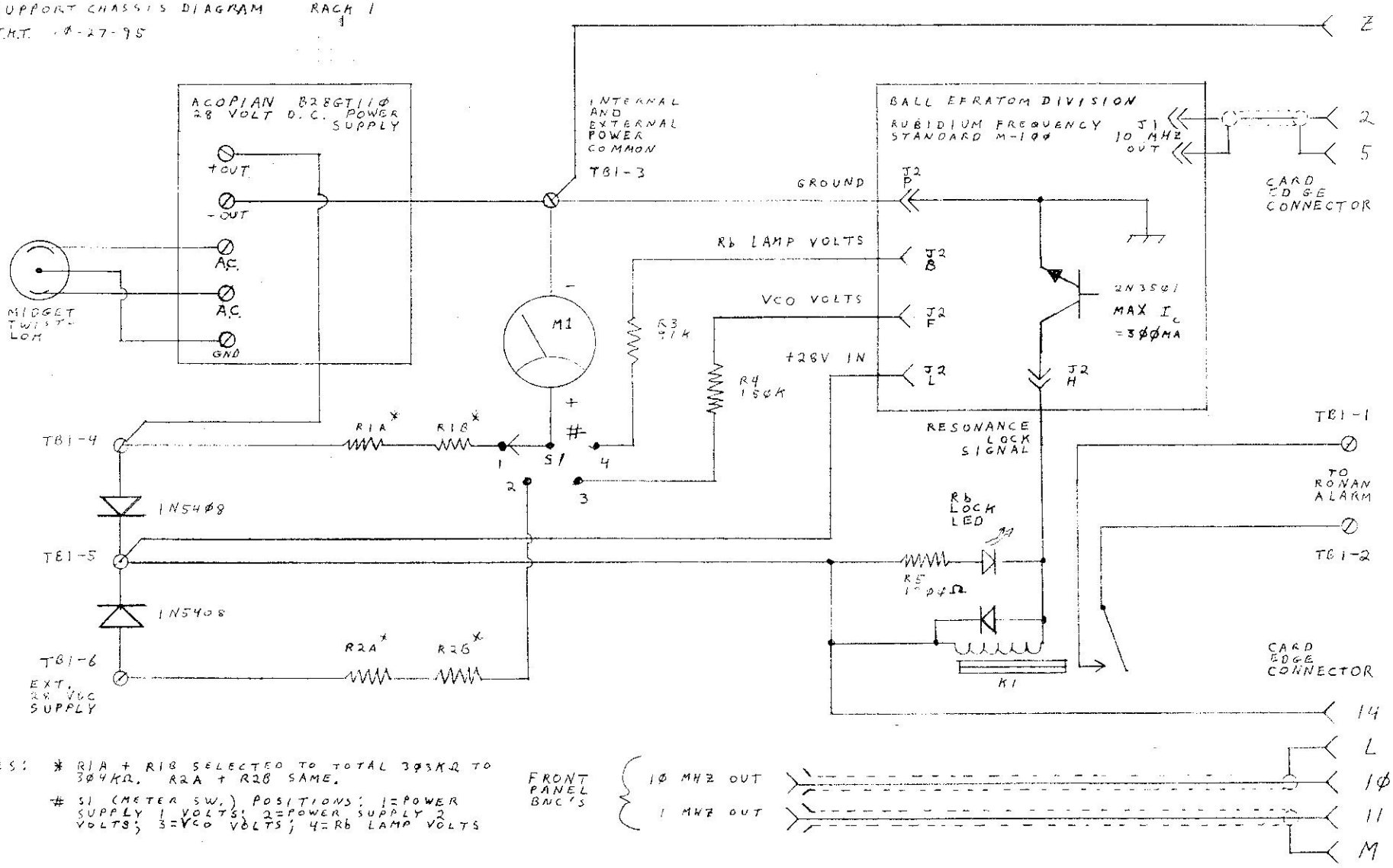
Capacitors C7 and C8 ensure a low impedance VCC source.

R11 is used to drop the applied voltage to regulator U4, thereby lowering it's dissipation and resulting heat load. Capacitors C9 and C10 ensure a low impedance supply voltage to U4.

KCBS-TV RUBIDIUM ATOMIC FREQUENCY STANDARD

SUPPORT CHASSIS DIAGRAM RACK 1

J.H.T. 10-27-95



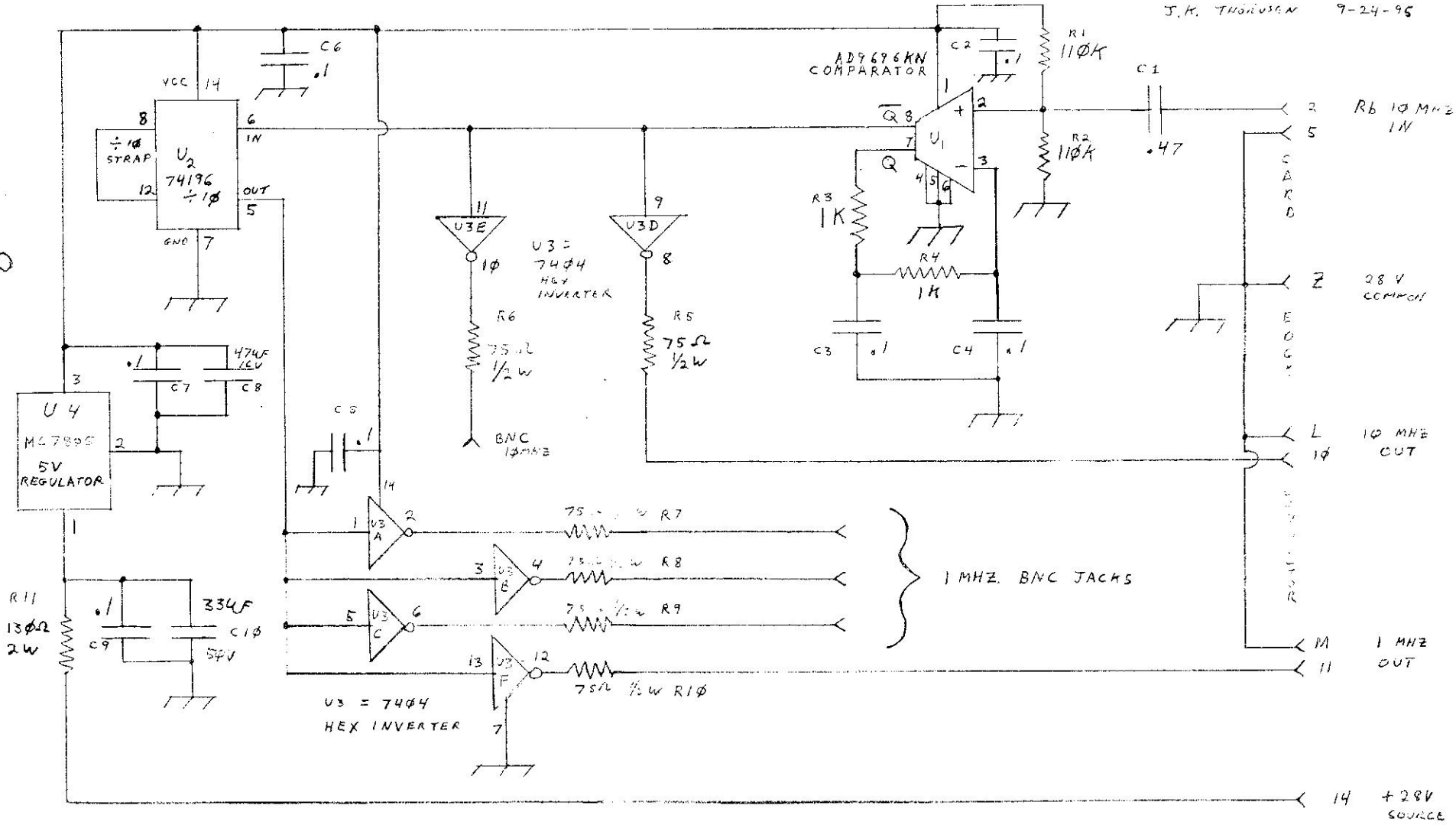
NOTES: * R1A + R1B SELECTED TO TOTAL 303KΩ TO 304KΩ. R2A + R2B SAME.

S1 (METER SW.) POSITIONS; 1=POWER SUPPLY 1 VOLTS; 2=POWER SUPPLY 2 VOLTS; 3=VCO VOLTS; 4=Rb LAMP VOLTS

RACK 1

KCBS-TV

ATOMIC FREQUENCY STANDARD
BUFFER AMP & DIVIDER CARD
J.K. THORVSEN 9-24-95



ENGINEERING CHANGE HISTORY

9-19-95 Changed design of interface card from block diagram A to block diagram B to provide 6 outputs instead of 4. Two extra outputs brought out to edge connector for connection to front panel sample BNC's.

9-21-95 Changed zero-crossing detector from design in schematic C to design in schematic D. Change effected to reduce variation in duty cycle of 10 MHz. square wave comparator output with change in input 10 MHz. signal level.

9-23-95 Added 120 ohm 2 watt resistor, .1 uF capacitor, and 33 uF capacitor. Resistor added ahead of MC7805 regulator to reduce regulator dissipation. Capacitors added to provide low impedance input to regulator. (See partial schematic E.)